CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A transceiver for processing high data rate serial data, comprising:

a first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial data, wherein the first clock data recovery circuitry receives the first serial data according to a first protocol;

a second clock data recovery circuitry for receiving second serial data and recovering a second recovered clock from the second serial data;

wherein the transceiver provides the first recovered clock, the second recovered clock, a reference clock, the first serial data and the second serial data to a plurality of clock based functionalities of the transceiver; and

wherein each of the plurality of clock based functionalities performs processing of one of the first serial data and the second serial data in accordance with a clock chosen from among the first recovered clock, the second recovered clock and the reference clock, and wherein at least one of the plurality of clock based functionalities converts the first serial data to a second protocol based on the first recovered clock and transmits the first serial data, as converted, in the second protocol based on the second recovered clock.

2. (Canceled)

3. (Previously presented) The transceiver of claim 1 wherein said second clock data recovery circuitry comprises a delay locked loop circuitry for receiving said second serial data and produces said second recovered clock from the second serial data, wherein the transceiver provides the second serial data to the plurality of clock based functionalities and wherein each of the plurality of clock based functionalities

uses one of the first recovered clock, the second recovered clock and the reference clock for processing of one of the first and second serial data.

4. (Previously presented) The transceiver of claim 1 wherein the first serial data is a receive serial bit stream.

5. (Previously presented) The transceiver of claim 1 wherein the plurality of clock based functionalities comprises a portion of a programmable logic fabric.

6. (Currently Amended) A transceiver for processing high data rate serial data, comprising:

a first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data, wherein the first circuitry provides the first recovered clock to a fabric comprising a first clock based functionality, a second clock based functionality, and a third clock based functionality, wherein the first circuitry receives the first serial data according to a first protocol;

a second circuitry for generating and providing a reference clock to the fabric;

a third circuitry for receiving second serial data and recovering a second recovered clock based on the second serial data, wherein the third circuitry provides the second recovered clock to the fabric; and

wherein each of the first, second and third clock based functionalities concurrently performs processing functions on one of the first serial data and the second serial data in accordance with a clock chosen from among the first recovered clock, the second recovered clock, and the reference clock, and wherein at least one of: the first clock based functionality, the second clock based functionality, or the third clock based functionality, converts the first serial data to a second protocol based on the first recovered clock and transmit the first serial data, as converted, in the second protocol based on the second recovered clock.

7. (Canceled)

8. (Currently Amended) A transceiver comprising:

a circuitry for receiving a plurality of input serial data streams, wherein the circuitry receives the plurality of input serial data streams according to a first protocol;

a clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams;

a circuitry for providing a reference clock; and

a logic for selecting from the plurality of input serial data streams and for providing at least one outgoing serial data stream to an outgoing transmit block;

wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing transmit block in accordance with a clock chosen from among the plurality of recovered clocks and said reference clock, and wherein the logic converts at least one of the plurality of input serial data streams to a second protocol based on a first one of the plurality of recovered clocks and transmits the at least one of the plurality of input serial data streams in the second protocol based on a second one of the plurality of recovered clocks.

9. (Previously presented) The transceiver of claim 8 wherein the outgoing transmit block is one of a programmable transmit physical media attachment (PMA) module and a transmitter port.

10. (Currently Amended) An integrated circuit, comprising:

at least one clock recovery circuitry coupled to receive a high data rate input data stream, wherein the at least one clock recovery circuitry recovers a plurality of recovered clocks based on the high data rate input data stream, wherein the at least one clock recovery circuitry receives the high data rate input data stream according to a first protocol; and

a programmable fabric portion comprising a plurality of clock based functionalities, wherein each of the clock based functionalities performs processing on the high data rate input data stream in accordance with a clock chosen from among the plurality of recovered clocks and a reference clock, wherein the programmable fabric portion converts the high data rate input data stream to a second protocol based

on a first one of the plurality of recovered clocks and transmits the high data rate input data stream, as converted, in the second protocol based on a second one of the plurality of recovered clocks.

11. (Previously presented) The integrated circuit of claim 10 wherein the high data rate input data stream is received according to a first protocol and is converted to a second protocol by the programmable fabric portion based on one of said plurality of recovered clocks.

12. (Previously presented) The integrated circuit of claim 11 further comprising a transmit circuitry coupled to receive the converted high data rate input data stream in the second protocol, wherein the programmable fabric portion provides the converted high data rate input data stream in the second protocol based on one of said plurality of recovered clocks.

13. (Previously presented) The integrated circuit of claim 11 wherein said at least one clock recovery circuitry comprises a second clock recovery circuit for recovering a second recovered clock based on an I/O serial data stream.

14. (Currently Amended) A method of processing high data rate serial data, comprising:

receiving a high data rate input data stream;

recovering a first recovered clock based on the high data rate input data stream;

recovering a second recovered clock based on a transmitter clock;

providing the first and second recovered clocks to a programmable fabric portion comprising a plurality of clock based functionalities; ~~and~~

performing processing of the high data rate input data stream in each of the plurality of clock based functionalities in accordance with a clock chosen from among the recovered clocks, wherein the high data rate input data stream is received

according to a first protocol and converted to a second protocol based on the first recovered clock; and

transmitting the converted high data rate input data stream in the second protocol based on the second recovered clock.

15. – 18. (Cancelled)

19. (Currently Amended) A method of processing high data rate serial data, comprising:

receiving a first serial bit stream and recovering a first recovered clock from the first serial bit stream, wherein the first serial bit stream is received according to a first protocol;

receiving a second serial bit stream and recovering a second recovered clock from the second serial bit stream;

providing the first and second recovered clocks and a reference clock to a plurality of clock based functionalities; ~~and~~

within each of the plurality of clock based functionalities, choosing among the first and second recovered clocks and the reference clock for processing of one of the first serial bit stream and the second serial bit stream by each of the plurality of clock based functionalities;

converting the first serial bit stream to a second protocol based on the first recovered clock; and

transmitting the first serial bit stream, as converted, in the second protocol based on the second recovered clock.

20. (Previously presented) The method of claim 19 wherein the first serial bit stream is a receive serial bit stream.

21. (Previously presented) The method of claim 19 wherein the second serial bit stream is a transmit serial bit stream.

22. (Currently Amended) A method of clock management in a processing block, comprising:

receiving a first data stream and recovering a first clock based on the first data stream, wherein the first data stream is received according to a first protocol;

providing the first clock to a fabric comprising a plurality of clock based functionalities;

receiving a second data stream and recovering a second clock based on the second data stream;

providing the second clock to the fabric;

providing a reference clock to the fabric; ~~and~~

concurrently performing processing functions on one of the first data stream and the second data stream in the processing block by choosing, by each of the plurality of clock based functionalities, a clock from among the first and second clocks and the reference clock;

converting the first data stream to a second protocol based on the first clock; and

transmitting the first data stream, as converted, in the second protocol based on the second clock.

23. (Currently Amended) A method for receiving and transmitting data, comprising:

receiving a plurality of input data streams, wherein the plurality of input data streams is received according to a first protocol;

recovering a corresponding plurality of clocks based on the plurality of input data streams;

determining at least one output port for providing outgoing data streams; ~~and~~

providing each input data stream of the plurality of input data streams to the at least one output port in accordance with a clock chosen from among the plurality of recovered clocks and a reference clock;

converting at least one of the plurality of input data streams to a second protocol based on a first one of the plurality of clocks; and

transmitting the at least one of the plurality of input data streams, as converted, in the second protocol based on a second one of the plurality of clocks;

wherein the at least one output port comprises a number of output ports that corresponds to a number of input data streams of the plurality of input data streams, and wherein the method further comprises determining, for each input data stream of the plurality of input data streams, an output port and providing each input data stream of the plurality of input data streams to the determined output ports based upon a chosen one of the plurality of recovered clocks and the reference clock.

24. (Canceled)